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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,049	01/20/2005	Jeong Il Byun	WA390/64724	3912

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EXAMINER	
MAYES, MELVIN C	
ART UNIT	**PAPER NUMBER**
1734	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/522,049	BYUN ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

(1)

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

(2)

Claims 1 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. 5,800,650 in view of Fuji et al. 2003/0064147.

Anderson et al. disclose a method of making a flexible multilayer printed circuit board comprising: providing laminates 35, 45 comprising a flexible substrate and conductive patterns 20, 22, 24, 26 (circuit boards), coating both sides of the circuit boards with a dielectric coverlayer 60, 62, 64, 66 to provide electrical insulation and environmental resistance, the coverlayers 62 ,64 provided over the conductive patterns 22, 24 to provide external access to the contact pads of the conductive patterns at a number of predetermined points; providing an anisotropic adhesive 70 of conducive particles in a thermosetting polymer between the circuit boards to provide electrical connection between the circuit boards; and laminating the circuit boards under heat and pressure. Anderson et al. disclose that the insulative coverlayers are provided on the circuit boards to a thickness of at most 50 microns, most preferably at most about 5 microns, depending on the amount of dielectric protection needed for the particular application. Anderson et al. disclose providing the insulative coverlayer 60 completely over the conductive pattern 20 to protect the circuit boards from the external environment (thus on a plain portion and a side portion of circuit patterns and on a bottom portion of a circuit board, as

claimed in Claim 8) while coverlayers 62, 64 which provide external access to the contact pads only partially cover the surface of the circuit patterns (thus on a side portion of the circuit pattern and a bottom portion of the circuit board, as claimed in Claim 9) (col. 7-16). Anderson et al. disclose providing the coverlayers 62, 64 to provide external access to the conductive patterns by screen printing or coating a dielectric ink followed by cutting apertures in the coverlayers at desired points but does not specifically disclose providing the dielectric ink as an insulating resin solution.

Fuji et al. teach that in the manufacture of a flexible circuit board having a resin coverlayer having no voids, the cover layer is formed by providing a resin solution, wetting the surface of the circuit substrate with a solvent, and applying and drying the resin solution [0007]-[0018].

It would have been obvious to one of ordinary skill in the art to have modified the method of Anderson et al. by providing the dielectric ink for forming the insulative coverlayers as a resin solution applied to the flexible circuit board after wetting the circuit boards with solvent, as taught by Fuji et al., to provide insulative coverlayers having no voids. The use of a resin solution for printing or coating on the circuit boards to form the coverlayers would have been obvious to one of ordinary skill in the art, as taught by Fuji et al.

Providing the coverlayers of thickness in the range of either 01.-5 microns or 0.3- 3 microns, as claimed in Claims 5 and 6, would have been obvious to one of ordinary skill in the art, as Anderson et al. disclose that the coverlayers are most preferably of thickness of at most 5 microns, depending on the amount of dielectric protection needed for the particular application,

thus suggesting to provide coverlayers of any thickness less than 5 microns as long as suitable dielectric protection is provided.

(3)

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. 5,800,650 in view of Fuji et al. 2003/0064147 as applied to claim 1, and further in view of JP 2002-179761.

Fuji et al. teach that the resin solution for forming a coverlayer of excellent insulation property can be provided by using a solution of resin or precursor of the resin, of resin such as epoxy resin [0018].

JP 2002-179761 (JP '761) teaches that an epoxy resin excellent in solvent solubility, excellent in heat resistance, moistureproofness and adhesiveness and useful as insulating material for circuit boards comprises an epoxy resin having a softening temperature of 63°C or more. JP '761 teaches providing epoxy resin of softening temperature of 71-85°C (Abstract and computer translation).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the resin solution as a solution of epoxy or precursor of epoxy, as taught by Fuji et al., as resin which provides a coverlayer of excellent insulation property, and to have provided the epoxy resin as a thermoplastic epoxy resin of softening temperature of at least 63°C, such as in the range of 71-85°C, as taught by JP '761, as epoxy resin excellent in solvent solubility, excellent in heat resistance, moistureproofness and adhesiveness and useful as insulating material for circuit boards. The use of a thermoplastic epoxy resin having a softening temperature in the range of 63-85°C, encompassed in the range as

claimed in Claim 2 and overlapping the range as claimed in Claim 4, would have been obvious to one of ordinary skill in the art, as suggested by JP '761 as epoxy resin of excellent properties for use as insulating material for circuit boards, thus useful for providing the epoxy resin solution for forming an insulative coverlayer.

Response to Arguments

(4)

Applicant's arguments filed June 9, 2006 have been fully considered but they are not persuasive.

Applicant argues that the dielectric coverlayers of Anderson et al. are not insulating resin solution and argues that Fuji et al. teach away from laminating a resin solution onto a circuit substrate using the heating and pressing lamination technique of Anderson et al.

(5)

Anderson et al. disclose screen printing or coating a dielectric ink on the circuit boards to form the coverlayers. Fuji et al. teach coverlayers for circuit board are formed without voids by forming the coverlayer by providing and applying a resin solution, thus suggesting to coat or screen print a dielectric ink comprised of a resin solution. Fuji et al. do not teach away from using rein solution for coverlayers when using heat and pressing to laminate circuit boards but only teach away from heat pressing a resin film onto a circuit board to form a coverlayer. The method of Anderson et al. is to apply a coverlayer to a circuit board by coating, the same as Fuji et al, not by laminating a preformed resin film by heat pressing.

Conclusion

(6)

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

(7)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
August 7, 2006